Eleven to Ten

Converting 27MHz CB sets to the 10 metre amateur band

by Bill Sparks G8FRX

To the comparative old timers; that is the early G8_____s and later G3_____s the present multitude of black, grey and blue boxes must often cause nostalgic reflections back to the good old days of their amateur beginnings. In the late 60s and early 70s the normal way of getting on the air was either by rolling your own or modifying government surplus gear or ex-commercial equipment. The early days of two-metre expansion (when 144MHz was opened to the Class B brigade) meant that the majority of rigs were ex-PMR, Pye, Storno, Cossor etc. Nowadays an all singing and dancing rig capable of working at least six repeaters via a linear and multi-element beam seems an essential requirement of the newly licensed G6_____, and the state of two-metre operating confirms this fact. Many operators must have longings for the good old days and those who have moved on to Class A have such an escape open to them, namely mobile FM on 29MHz.

With the advent of CB, equipment capable of easy modification to 29MHz is available cheaply. Some of the transceivers around are of a reasonably high standard, giving scope for modification to good performance at very low cost. Cheap mobile aerials are also readily available.

40 channels

A typical block diagram of a 40 channel (10kHz spacing) CB set would be as in **Fig. 1.** For simplicity an AM set is chosen. Details on converting an AM set to FM (with a performance typical of 145MHz gear) will be given later.

The basic transmitter and receiver circuits are fairly conventional in that a low power PA is driven by a simple driver, both stages being modulated. The predriver stage is excited by a frequency synthesiser which also includes a safety circuit. This cuts the transmitter off if the synthesiser goes out of lock. The synthesiser consists of a voltage controlled oscillator operating (in this case) at the output frequency minus the first IF (generally 10.695MHz). The synthesiser is locked to a multiple of 10kHz, derived from 10.240MHz crystal. This 10.240MHz oscillator circuit also drives the second receiver mixer, giving a second IF of 455kHz. The VCO frequency is mixed with the 10.695MHz oscillator to transmit on the same spot as the RX input frequency. Suitable T/R switching is provided and the rig operates like just about any other transceiver. The main difference between the conventional amateur arrangement and the one discussed above is that the injection frequency to the first RX mixer is lower than the received channel, whereas it is normal amateur practice to operate receiver oscillators on the high side of the signal frequency. The variety of CB equipment is extremely wide but certain basic similarities are found. The major variations are in the frequency synthesisers. Since our aim is to transfer the operating frequency to a point some 2MHz higher we will consider the synthesiser stages first.

Basically, there are three main techniques used in synthesiser circuitry in CB sets although certain other oddball circuits exist. The three methods are as follows:

a) To prevent any form of conversion to additional frequencies a form of Read Only Memory is incorporated in the PLL whch is dedicated to giving only the forty channels recognised by the FCC in America. Typical devices are the (see Appendix 1) 7137, 7130 and 7131. These devices are invariably operated by programmed input lines usually by a 6 bit code.
b) Another form of pre-programmed device uses a so called 'random' code which is a variation of the 7 bit BCD code, eg. 9106 & 9109.
c) The major proportion of the sets used phase locked loop circuits controlled by a straight binary input and these are comparatively simple to re-tune. A brief explanation of binary arithmetic is given in Appendix 4.

Dedicated v binary

In type (a) & (b) the device is

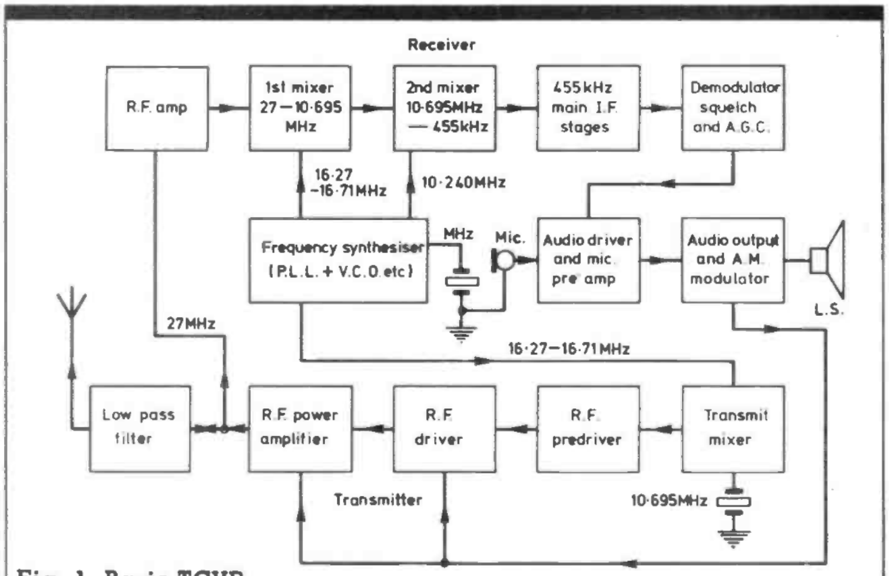


Fig. 1. Basic TCVR

usually loaded with forty discrete operations and these are called up by the input logic variation, but in type (c) the number of operations carried out by the device is controlled only by the binary number range the device will accept. In many cases as many as nine inputs or program lines are available, thus giving 2^9 variations, ie. 511 different lines. Since we originally stated that the channelling was at 10kHz intervals this gives a tuning range of 5.11MHz.

The simple operation of a synthesiser PLL circuit is shown in **Fig. 2**. When the reference frequency f_r and the VCO frequency f_o are applied to the phase detector, the phase difference is measured in the phase detector and converted into a DC output which is applied to the VCO via the low pass filter. Since the comparison is made every cycle there will be harmonics and noise at the output P, hence the need for the low pass filter. The integrated DC voltage applied to the VCO causes a frequency change to occur, the VCO output being returned to the phase detector. The closed loop will continue to operate until there is no phase difference between the voltage generated in the VCO and that of the reference. The VCO is then locked on to the reference frequency and the VCO output (f_o) is in phase lock with the reference.

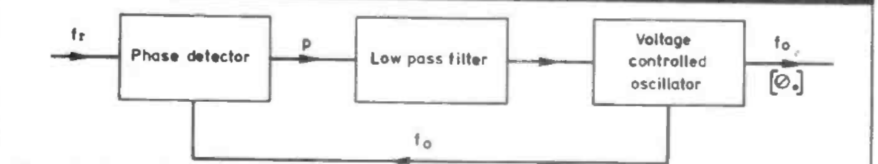


Fig. 2. Simplified phase lock loop.

To apply this technique in real terms some additional sophistication is required. Since variable frequency dividers used in these circuits have a fairly low frequency maximum count limit and we require a 10kHz channel spacing we have to accept that we are referring to a 10kHz reference and that our VCO frequency of approximately 17MHz has to be divided by some 1700. To overcome this problem the VCO frequency is mixed with an offset oscillator, to give a lower variable frequency which does not require such a high division ratio. **Figure 3** indicates a fully operational arrangement.

In order to achieve a range covering 29+MHz it is necessary to alter VCO to give 29.5-11.695MHz as the operating range.

In the example quoted the channel switch on channel 1 gives an output code of 136, so our new frequency on 29MHz at the lowest end of the range should be controlled by a 136 programmed input to the PLL to be used. By substituting a 17.245 crystal for the 14.910 crystal in the original circuit our transmit frequency should now be between 29.300 and 29.700. However, due to FCC regulations, the original FCC frequency allocation to CB had certain discrete gaps at 50kHz intervals. The channel switches were designed to skip these numbers in their output; so a typical output sequence from the switch used in our example would be 136, 137, 138, 140, 141, 142, 143, 145, 146, 147, 148, 150 and so on up to channel 20, where normal sequential counting took over up to channel 22. Channel 23 required a count of 165, whereas channel 22 was 162. The sequence at this point was channels 22 — 24 — 23 — 26; then normal counting up to level 44 or in our instance 180.

By interrupting the program lines from the switch and feeding them via a suitably programmed EPROM the necessary corrections can be made to the coding, so that the switch reading 1-40 gives a progressive binary input to the PLL, enabling a true 10kHz channel sequence.

In some instances the VCO coil may not tune to the new frequencies. This can be changed fairly easily either by reducing the length of the coil or by reducing the coil padding capacitor.

Where it is necessary to replace the synthesiser due to it being a dedicated device, the simplest method is to introduce a composite board containing the EPROM and the alternative synthesiser. A suitable board is shown in **Fig. 4** together with the circuit and layout in **Figs. 5 & 6.** As the circuit indicates the program lines are fed to the EPROM and the modified program is then fed to the synthesiser. The details of operation and installation will be dealt with later in the article.

PCB drawings Figs. 4, 6 and 9 will appear in a future issue. Unfortunately there were mistakes in the original artwork — Ed.

Another technique was often used to cut the number of crystals. By taking the 10.240MHz signal and dividing it by two, a 5.12MHz signal was derived. This frequency was multiplied by three to give 15.36MHz which was then mixed with the VCO. This was then submitted to the divide-by-N module, giv-

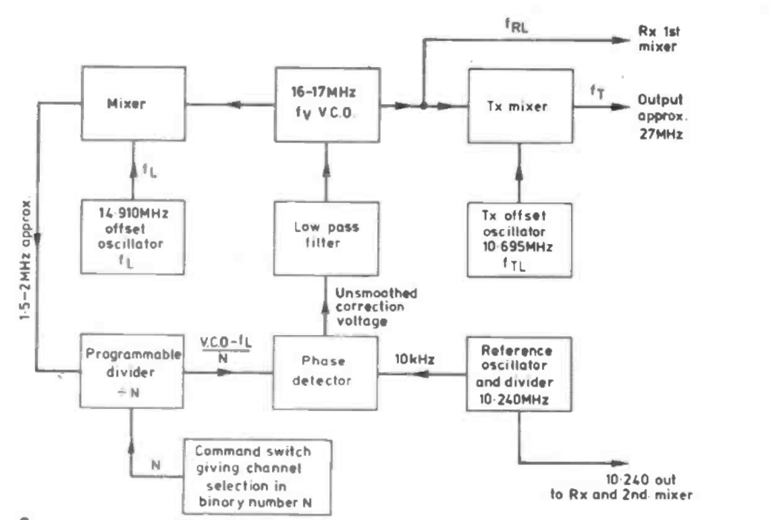


Fig. 3. Typical synthesiser arrangement.

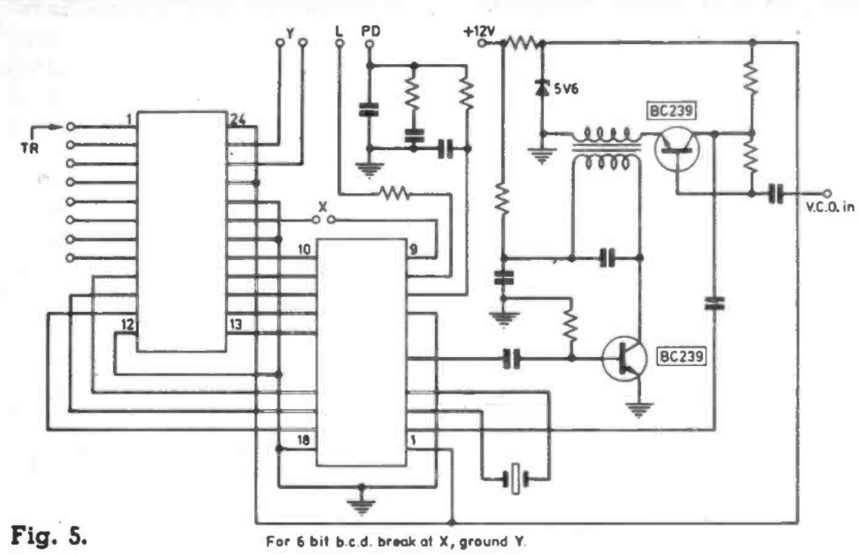


Fig. 5.

For 6 bit b.c.d. break at X, ground Y.

ing a count range similar to the ones discussed previously.

From the discussions so far it would appear that the majority of sets around could be converted to operate on 29MHz FM.

The use of the 10.240MHz crystal as the reference oscillator permits a variety of functions.

a) The division by 2^{10} gives 10kHz since 2^{10} is 1024.

b) Division by two and multiplication by three gives 15.36MHz which is a handy offset frequency, also multiplication by two gives 20.480MHz, also a handy offset frequency.

c) The technique adopted in nearly all the units is to operate the VCO at either (input frequency + 10.695MHz) or (input frequency minus 10.695MHz), 10.695MHz being the value chosen for the first IF. By mixing this 10.695MHz with 10.240 in the second oscillator the standard 455kHz IF is produced.

Referring back to our original comment on (b) above, the device chosen for the alternative synthesiser was a Motorola device MC145106. This operation of this device is shown diagramatically in **Fig.8.** The particular device used has an effective counting range of 10^9 ($2^0 - 2^8$) or some 512+ in binary steps. The technique finally adopted is to count in units of two, ie. 2, 4, 6, etc. and to utilise the 5kHz split so that each step is 10kHz (ie. 2 x 5kHz). However by switching internally the device can count in even pairs, ie. 2, 4, 6, 8 etc., or in odd pairs, 1, 3, 5, 7 etc. This technique allows for the 455kHz receiver IF. This is now derived by programming the device to read 91 steps which at 5kHz intervals is 455kHz and then mixing this with the 10.240 frequency to achieve the required output in the T/R switching.

ie. VCO + 455kHz + 10.240MHz = TX frequency

In practical terms the VCO output is fed to a simple transistor mixer which is hard switched by the 15.36MHz derived as shown in the circuit diagram for the board, **Fig.4.**

The two devices shown at the input to the dividers are Schmitt triggers, which assist in preventing random noise from operating the counters, by squaring the shape of the input pulses. In the case of conversion to MPT1320 the 5kHz technique permits a frequency shift of a straight 64 in count (27.605 — 26.965) and then 5kHz correction of the 27.605 to bring it to 27.600. A slight tweak to the 10.240 crystal then brings the resultant frequency to within 1-200 cycles of 27.60125. Similar techniques will permit the

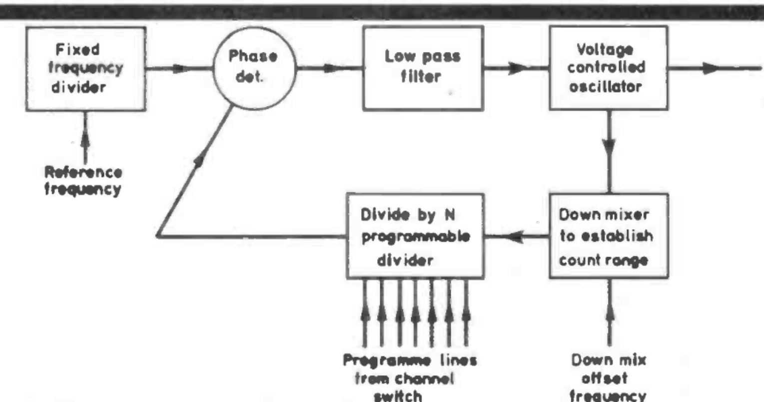


Fig. 7. Characteristics of straight synthesiser.

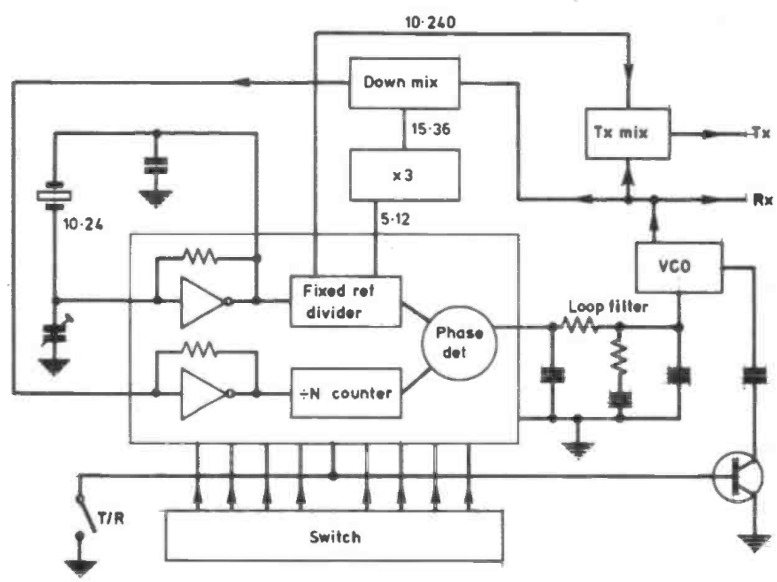
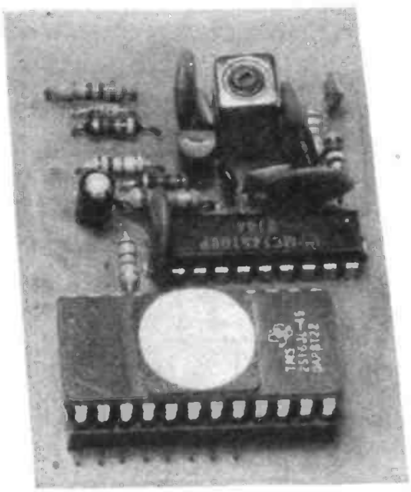
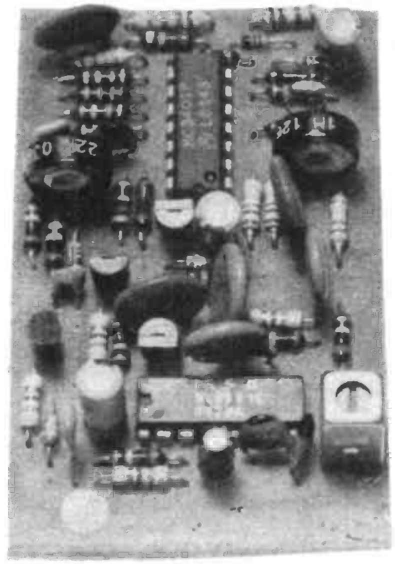


Fig. 8. Technique used in circuit adopted (MC145106)

circuit to operate at any required frequency within the capabilities of the counter and the VCO. To remove the gaps on the FCC sets, suitably programmed EPROMs could be used as follows. In the case of the sets using the straight binary input PLL where the original synthesiser can remain in situ, the technique adopted is to cut the tracks from the switch to the device, and feed the program lines from the switch to the input lines of the EPROM via the address lines, remembering to keep the lines in the correct order. See **Fig. 9.**

In the EPROM used on the board shown in **Fig.4** the least significant digit is fed to address line 8 and the most significant to address line 3 in the case of 6 bit BCD. Address line 2 is used as the T/R line to introduce the offset of 455kHz in the specific program on this EPROM but in the case of straight binary, address lines 8 — 1 are used as inputs. A suitable board layout for the code transfer is shown **(Fig.9)**. This provides a facility for introducing a 5V regulated supply. It will be found in many cases that the leakage at the input of the EPROM address lines is so low that static charges can build up. It is therefore advisable to install pull-down resistors (50K — 500K 1/8 watt), across the wide earth line in the centre of the board. (Shown in **Fig.9.**





The loop filter shown in the diagram of the 145106 devices is important and due to its critical nature, when the system is being used as an alternative to dedicated device it is important to completely isolate the original loop filter to avoid incompatibility problems.

In order to explain the technique still further perhaps a look at a typical binary indication would help. In view of space restrictions only certain channels will be shown but the sequence, being additive should be easily followed as indicated in **Table 1.** (For further information on binary codes see appendix 3).

In the first example a difference offset frequency in which the VCO would be operating in the 36MHz region is shown. The offset frequency could be derived from a crystal oscillator operating around 37MHz or the circuit could use a 17MHz VCO with the 10.240 crystal oscillator being doubled to 20.48MHz if mixed with the 17MHz VCO this would give a down count for an increase in VCO frequency. Both techniques are used.

Table 1

	Code	256	128	64	32	16	8	4	2	1	Powers of 2
Frequency	Sum	7	8	9	10	11	12	13	14	15	Pin Number
27.601	74	0	0	1	0	0	1	0	1	0	Using pins
9-15 only with											
27.701	64	0	0	1	0	0	0	0	0	0	down count
technique											
27.801	54	0	0	0	1	1	0	1	1	0	
	256	1	0	0	0	0	0	0	0	0	Using all pins 7-15
	257	1	0	0	0	0	0	0	0	0	and up count
	260	1	0	0	0	0	0	0	0	0	
	511	1	1	1	1	1	1	1	1	1	
26.965	136	0	1	0	0	0	1	0	0	0	Pins 8-15
27.605	200	0	1	1	0	0	1	0	0	0	" "
27.995	239	0	1	1	1	0	1	1	1	1	" "
29.605	400	1	1	0	0	1	0	0	0	0	Pins 7-15

The interesting point is that the 40 positions on the channel switch can be placed at any point between the count of 1 and 511, this giving a frequency coverage of over 5MHz with a 10kHz channelling or 2.5MHz+ with 5kHz channelling. The important feature to recognise is that the code lines from the switch should not over-range the available program range. In other words the use of six program lines will only permit a count range between 63 and 0 so if the switch gives out 136

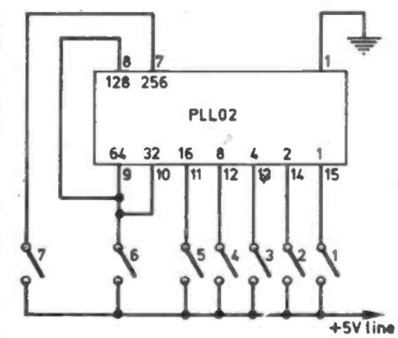


Fig. 10.

— 174, the range must include eight input lines. A simple device could be shown as in **Fig.10.**

By closing switch 6 we have a pre-loaded count of 224 already in the line, using switches 1 — 5 gives us a count range of 31, so we have now an effective range of 224 — 255. By closing switch 7 and opening all the other switches we now have 256 count. By progressing through switches 1 — 5 gain with 7 closed we can now count to 287 so that in effect using the above technique we have a count range of 224 — 287, so 64 positions are open to us in this instance from the combinations of switches 1 — 7, and the 64 positions can be seen anywhere up to 511, ie. the 640kHz swing can be at any point in a 5MHz range. As can be seen we have pre-loaded 224 so that it becomes obvious that by pre-loading any quantity up to 256 we can set our operating range to suit, but in order to cover certain areas we may have to arrange an intermediate switching of the loaded point.

The practical operations involved are relatively simple and by using EPROMs to carry out the mechanical operation just described the techniques are well within the skill of the average amateur. The main problem is in the programming of the EPROMs. The important feature is to establish the program already being fed to the EPROM by preparing a truth table on the pattern shown for the MC145106. It is only necessary to check the code at channel 1 and channel 40, the rest can be calculated. The technique for establishing the code pattern is to check the voltage level on each of the program lines in turn at the selected channel switch position. A voltage of some five volts indicates a logic 1, and any voltage less than 0.5 indicated logic zero. It is advisable in these cases to use an analogue meter of some 20,000 ohms per volt to present a suitable load otherwise random static voltages may affect the readings.

In discussing the practical operation probably the most suitable manner would be to use one of the most common circuits. The one chosen is used by a variety of manufacturers and is given in **Fig.11.** The VCO control voltage is derived from pin 17 and goes via R201, C203 and R204 to the varicap diode D201 which is across the coil L203. C304 serves as the DC isolating cap and has a loading effect on frequency range, so being in series with the varicap controls the VCO operating range. The KC7310 device acts as the transmit mixer and VCO. The VCO output is tapped off at pin 2 of the 7310 and fed via C305 to the PLL, in this case a 7131. The VCO return via C305 is red to pin 19 of the PLL and in the PLL is fed to the programmable divider. This is controlled by an internal ROM and this ROM accepts the input lines from the channel switch (pins 1 — 6 incl.).

The T/R line instructs the internal ROM to read the offset and consequently moves the VCO frequency, as discussed previously. A certain amount of the RF is fed back to the PLL via pin 14 as a lock check and an out-of-lock indication causes the device to inhibit, this preventing any off-frequency transmission.

The channel switch controls the digital information to the device and at the same time this information is fed to the digital display.

The techniques required to override the synthesiser shown and to vary the output frequency to a previously determined range are all accomplished on one board. **(Fig.4)** This board accepts the incoming information and takes over control of the VCO in the following manner.

The program information is fed to the EPROM and this transforms it to an acceptable code for the PLL used. The control functions are taken over as per the layout shown for the device and the actual circuit used is shown in **Fig.4.**

The physical operations involved are to lift the end of R201 adjacent to TP1 and clear it from the board. Run a wire from Pin 7 on the new board (shown as output on diagram) to this resistor. The 10.240 crystal is removed and soldered on to the new board together with the 56pF capacitor. The other capacitor is replaced on the new board by a 33pF cap. The program lines are removed from pins 1 — 6 on the old board and inserted in pins 8 — 3 on the new board. A T/R line point is taken from the junction of R316 and diode MA150 (D209) and fed to pin 2 on the new board. The 12V point is fed from the set side of the on/off switch and a suitable earth connection made. The VCO return is taken from pin 2 of the 7310 mixer by first removing C305 and taking the wire from the 7310 side to the new board. The inhibit line is disabled by cutting the track at pin 14 on the 7130.

By connecting a voltmeter between pin 8 of the new board and earth the conversion should be complete. Initially set the channel switch to channel 20, then adjust the VCO coil until a voltage of some 5V appears at pin 8. This voltage should stay at 5 volts when the channel switch is moved from 1 — 40. This indicates that the circuit is in lock throughout the new frequency range. In the case of difficulty the check points are as follows:-

a) Check on pins 2 & 3 of the 145106 to ensure that the 10.240 oscilator is working.
b) Check pin 5 for 5.12MHz output.
c) Check at mixer transistor for 15.36MHz, if not present adjust tripler coil to give a maximum of 15.36MHz output (core flush with top of can).
d) Ensure that EPROM is receiving 5 volts and no more.
e) Check that T/R line is switching.
f) Ensure that VCO return is present.

The actual RF voltages as shown on a scope should be in excess of 0.6 volts in case of the RF return from

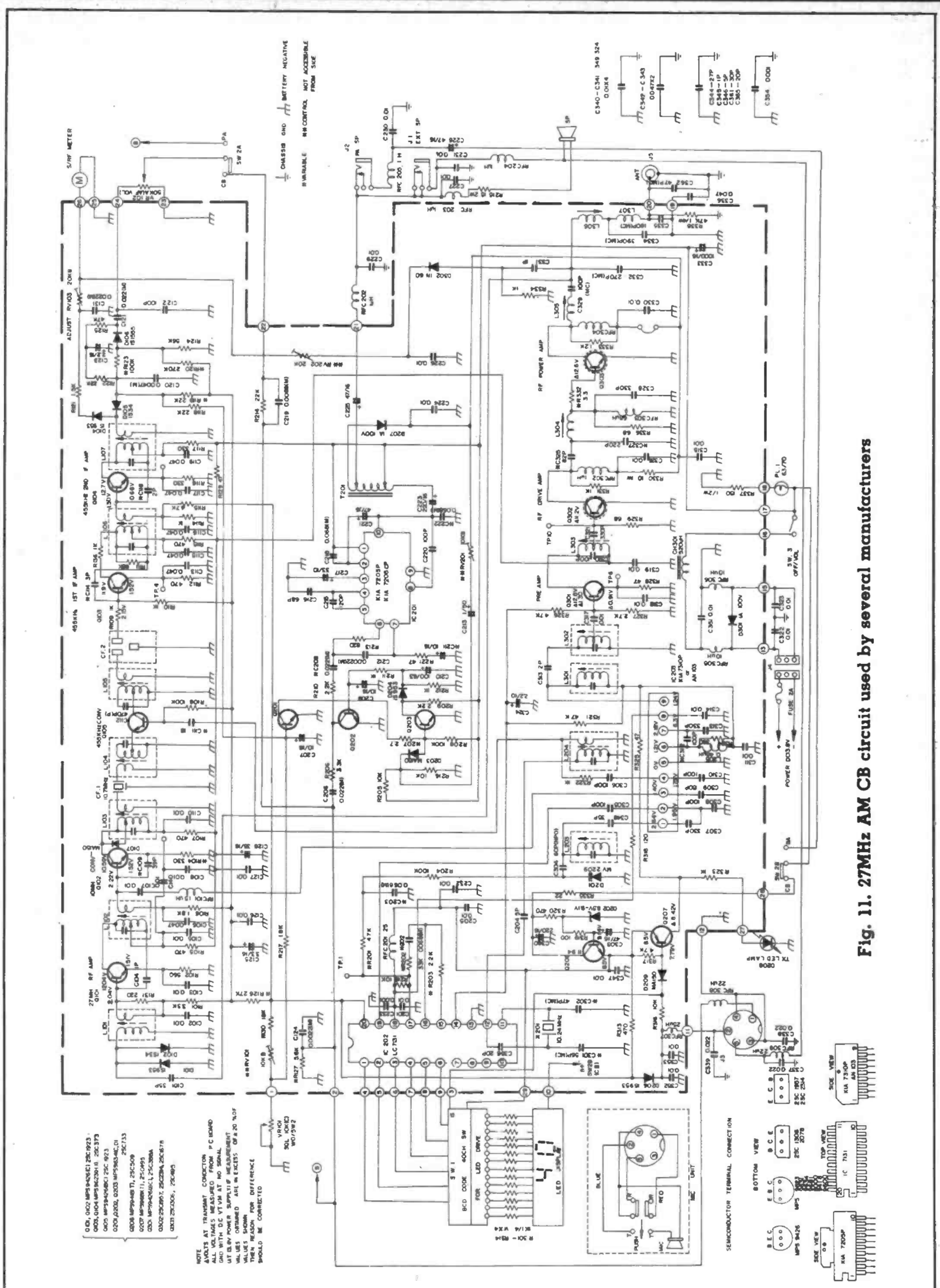


Fig. 11. 27MHz AM CB circuit used by several manufacturers

the VCO and the 15.36MHz injection to the mixer on the board as shown in the appendix.

Various techniques are available for a variety of circuits but all follow the basic arrangement as outlined above. The stability attainable is well within required standards and is more than adequate for normal requirements.

To convert the AM to FM operation is again a straightforward task. A small FM modulator circuit is introduced in which the microphone input line is lifted from the board at point 2 and inserted into the modulator/discriminator board. The modulator used consists of a quad operational amplifier in which the first stage includes an adjustable gain stage followed by a diode clipper and a filter network using one active and two passive filters. The circuit and board layout for the modulator is given in the appendix and the output from the varicap point is applied to pin 2 of the 7310 when it is in effect in parallel with the VCO via the bridge of C308/C307.

The pre-emphasis achieved is some 6dB per octave and the first low pass filter give a roll-off of some 6dB per octave after about 2,800Hz. The other filters give an additional roll-off of some 12dB per octave so the audio response is as in **Fig.13**.

The effect of using an adjustable gain stage in the initial part of the circuit followed by an amplitude limiter is to give a sensibly constant audio output over a range of inputs from some 20mV to 200mV. In effect the design operates as a very efficient speech processor with a high degree of distortion reduction at the output, and the audio quality obtained is of a very high standard indeed. The design is based upon a Motorola concept drawn around their MC3401 device, which operates very effectively at 9 volts.

The low capacitance added to the VCO by the varicap is compensated for by the control voltage so that at resting frequency the desired frequency is not pulled and audio variations across the diode cause a good quality FM signal to be created. The only setting up required is to advance the input pot to just below clipping level and to set the output pot to the required deviation level. In some circuits the amount of VCO swing may not be sufficient and in this case the output from the deviation control may be fed by a 1 μF electrolytic to the TP1 connection at R201. In this case the deviation will require stepping down on the pot since it is now possible to get up to 15kHz deviation. The signal sounds very loud but could be frowned upon! Alternatively the 100k resistor in the input could be by passed.

An audio oscillator of some 50mV output at 1500Hz connected to the mic input line acts as a suitable check for setting the deviation. Nor-

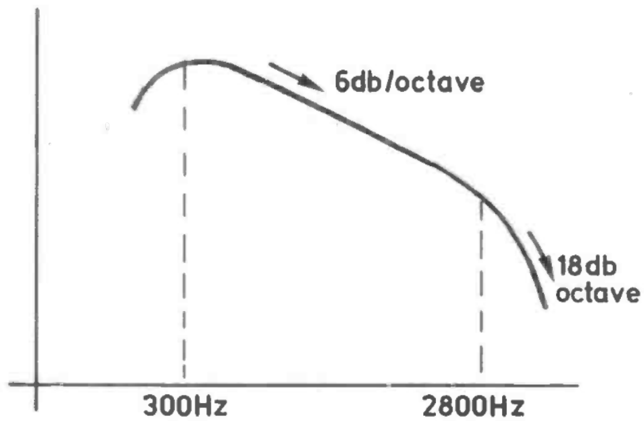


Fig. 13. Tailored audio response to achieve optimum value of modulation index at nominal 3.5kHz deviation max.

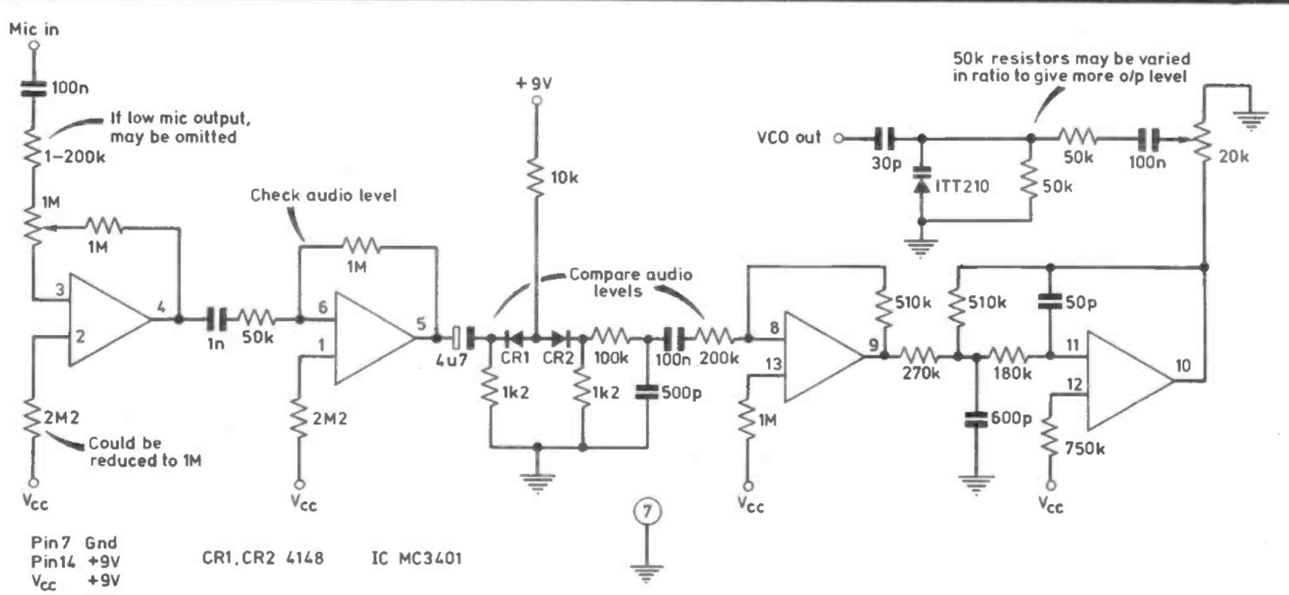


Fig. 12. Modulator circuit used.

mally it is not necessary to remove the modulation transformer but if desired C225 should be changed to 200uF, and a bridge taken from C223 to C225. The 12V line can then be taken across the original pins of the transformer from the 12V line to the diode D207.

In the receiver the IF output is taken from the base of Q104 (secondary of the IF transformer) direct to the board via a screened lead, the screen acting as the earth return. The audio output is then taken to the top of the volume control after lifting the wire from the C121/C122 function. This removes the AM detector from the circuit but allows the AGC and squelch to operate and keeps the signal meter in circuit.

The device used in the discriminator is the Plessey 6691, a high quality quadrature detector with its own built-in pre-amp and audio circuit. The audio output is adequate to drive the normal AF amplifier devices found in the sets commonly used and gives an extremely good performance with a high degree of AM rejection.

The use of a modulator and discriminator on the one board requires a degree of separation on T/R since the modulator can create audio oscillation if allowed to operate on receive. Accordingly, a T/R switching network which switches the modulator on and the discriminator off during transmit and vice-versa on receive is used. The T/R line operating this function is derived from the coil side of R325. Due to circuit conditions a certain residual voltage is present on this line in the off position so the 3V zener in series with the line at the input to the board ensures that at least 3V must appear before the circuit switches.

Prior to this the residual voltage was capable of leaving the modulator on during receive.

For anyone wishing to convert an AM to set to the HO MPT 1320 condition, the above conversions are acceptable to the HO and providing a Customs clearance form is filled in and the relevant fee paid a set infinitely superior to the majority of the so-called FM sets on the market today can be produced. It is easy to recognise a properly converted set since the audio quality is so superior to the normal 'muppet box'.

The discriminator shown can only operate at IF values up to 1.5MHz or so and a suitable circuit and board layout for a higher IF using a Plessey 6600 is shown in **Fig.14**. In this instance the use of tracking oscillator techniques gives a superb AM rejection and very good interference suppression since only frequency variations are recognised. By reducing the IF to 100kHz a good audio output level can be achieved.

The AM rejection of the discriminator normally used is very good and the only adjustment required is to adjust the core of the quad transformer for maximum readability on the FM signal. This automatically gives the best AM rejection. Final adjustments are to peak the RX front end to 29MHz and retune the TX stages to the new frequencies.

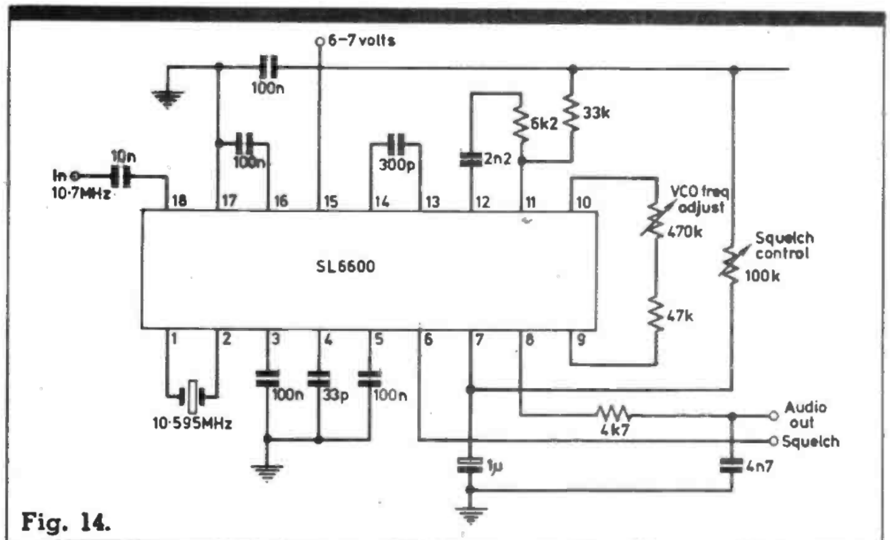


Fig. 14.

The only other consideration is the poor front end and early IF stages performance of the usual receiver. By changing the front end RF transistor for a more suitable type (choose one suitable for use up to 150MHz) with a slightly lower gain the cross modulation performance can be substantially improved. The normal ceramic 10.7MHz filter installed can also be changed for a crystal filter (costing from £3 — £6) with marked effect on adjacent channel performance. The crystal filters have centre frequencies of 10.695MHz. Appendix 1 shows the breakdown into types of most of the PLL devices commonly used. In some cases combinations of devices are used as in the Sharps series, where a divider is separate from the phase detector. In the Sharps (probably the best of the older CB sets) the mixing technique uses two 11MHz crystals for transmit and receive offset. When the count conversion is carried out by simply lifting the grounded 64 pin and putting it to logic 1 the frequency automatically moves up 640kHz. In order to bring the 4.75kHz required to meet MPT 1320 into operation, simply cut the track alongside each crystal and place a 27pF cap across the break. This shifts the crystals by about 4.75kHz.

The codes used in three different devices are shown in **Fig.15.** Only channels 1, 10, 20 and 40 are shown to illustrate the code sequences but the patterns should be obvious from the sequence shown.

Device	2^n	= →	64	32	16	8	4	2	1	
	Channel No	Code Sum	IC pin No 9	10	11	12	13	14	15	
PLL02A pins 7&8 high	1	74	1	0	0	1	0	1	0	
	10	63	0	1	1	1	1	1	1	
	20	50	0	1	1	0	0	1	0	
	40	30	0	0	1	1	1	1	0	
			7 bit straight binary							
	Powers of 2^n →		4	2	1	8	4	2	1	
	Pin No →		13	14	15	2	3	4	5	
MSC42502 pin 12 high	1	0·1	0	0	0	0	0	0	1	
	10	1·2	0	0	1	0	0	1	0	
	20	2·5	0	1	0	0	1	0	1	
	40	4·5	1	0	0	0	1	0	1	
			7 bit binary coded decimal							
	Powers of 2^n →			2	1	8	4	2	1	
	Pin No →			6	5	4	3	2	1	
LC7120	1	0·1		0	0	0	0	0	1	
	10	1·0		0	1	0	0	0	0	
	20	2·0		1	0	0	0	0	0	
	40	0·0		0	0	0	0	0	0	
			6 bit binary coded decimal							
	Powers of 2 not used in logical sequence									
	Pin No →		17	16	15	14	13	12	11	10
TC9109	1		1	1	1	1	1	1	1	1
	10		1	1	0	0	0	1	0	0
	20		1	0	1	0	0	1	0	0
	40		0	1	0	0	0	1	0	0
			8 bit random code							

Showing code distribution in different modes

Fig. 15. Powers of 2

And attempt has been made to bring about three objectives:

a) To stimulate interest in building something yourself at low cost.

b) To create activity on 29MHz before someone moves in because of lack of operation on the band.
c) To find a use of discarded CB sets now that new reforms are being introduced more stringently.

With minor variation the above techniques have been applied to SSB rigs in an effort to simulate mobile activity on 10 metre SSB.

Many CB aerials can be retuned to 28-29MHz with little difficulty and a host of reasonable test gear at very cheap prices is also available.

To date some 2 — 3000 conversions to 27MHz FM have been made to a variety of sets and basically the same technique applies to 29MHz.

Appendix 4

Binary Arithmetic

Binary arithmetic is an arrangement of numbers in ascending powers of two.

The standard arrangement is as shown in the table across the page (below).

Power of 2	0	1	2	3	4	5	6	7	8	9	10	11	12	2^n
Binary No.	1	2	4	8	16	32	64	128	256	512	1024	2028	4056	Code sum
Sample	0	1	0	1	1	1	0	0	1	1	0	0	0	826

As can be seen if each level could be selected and shown as being used by indicating as 1 whereas unused lines were indicated as 0 then any number between 0 and 8111* could be shown by using the above sequence. A typical arrangement showing a count of 826 is shown, ie the sum total of 512, 256, 32, 16, 8 and 2.

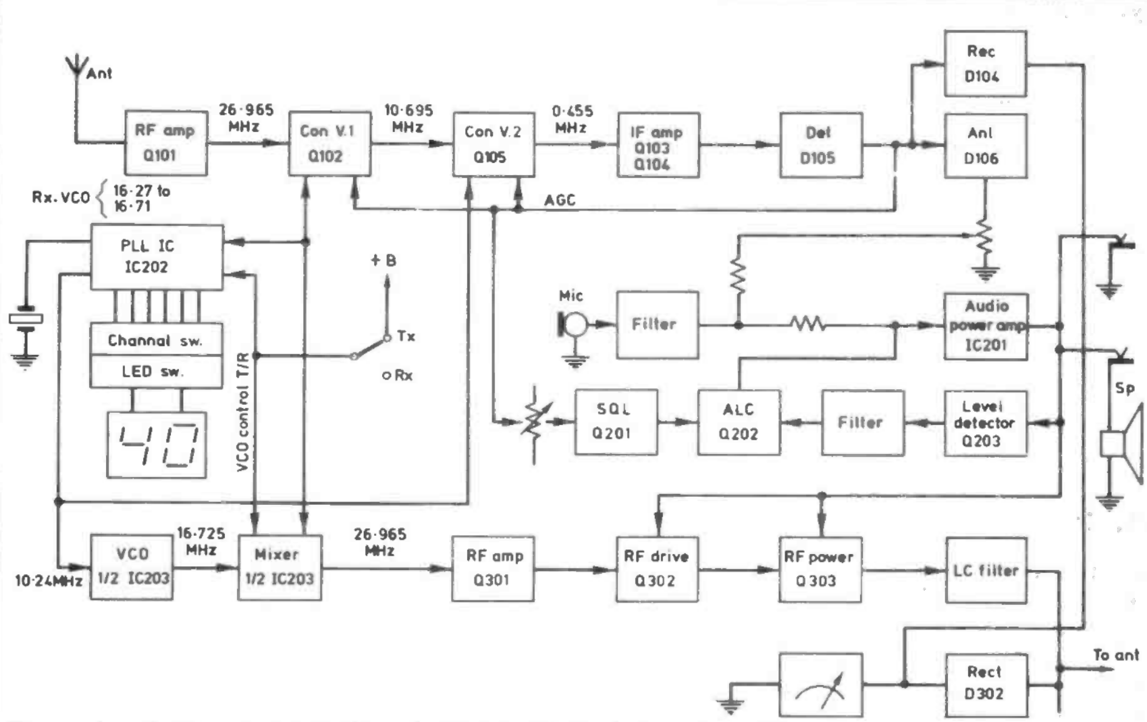
*8111 = sum of all values shown from 4056-1.

This system is known as straight binary. One other form is used in the systems discussed in the article ie. Binary Coded decimal or BCD. In this case only symbols up to 2^3 are used as number indicators, either two or three additional channels are used as decimal point indicators, and multipliers.

Appendix 1

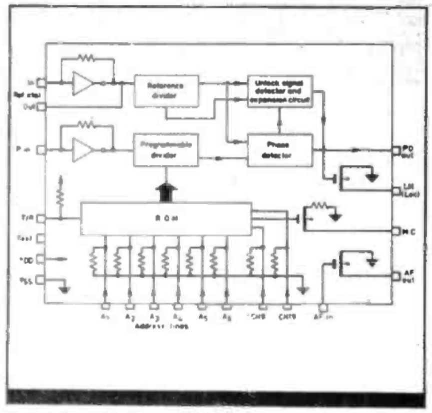
Codes Used in Various P.L.L. Devices

Binary Inputs	Binary in Internal ROM	BCD in BCD Code Convertor	Programme Inputs	Random Code
CC 13001	LC 7110	LC 7120	LC 7130	TC 9106P
CC 13002		UPD 861C	MSC 42502P	TC 9109P
LC 7113		UPD 2810C	UPD 858C	
MC 58472*		UPD 2812C		
MC 58473P		UPD 2814C	LC 7131	
MB 8719		UPD 2816C	LC 7135	
MB 8734		LC7137		
MC 145104				
MM 55104				
MM 55114		Require		Require
MM 55124		Synthesiser		Synthesiser
MN 6040 A		Replacement		Replacement
SM 5104				
MC 145106				
MM 55106				
MM 55116				
MM 55126				
MM 55108				
SM 5118				
MC 145107				
MM 55107				
SM 5107				
MC 14568				
MC 14526				
MC 145109				
PLL02A/AG				
SM 5109				
TC 9100P				
MSM 5807				
MSM 5907				
MDC 40013				
NIS 7261A				
NIS 7264B				
PLL01A				
PLL03A				
REC 86345				
TC 5080P				
TC 9102P				
TC 9103P				
PLL08A				



Appendix. 2. Showing circuit path of tranceiver chosen as sample

Power of 2		3	2	1	3	2	1	0	2^n
Binary No.	Code sums	4	2	1	8	4	2	1	Code sum
Sample	0.6	0	0	0	0	1	1	0	6
numbers	1.6	0	0	1	0	1	1	0	16
shown	2.6	0	1	0	0	1	1	0	26
	3.6	0	1	1	0	1	1	0	36
	4.6	1	0	0	0	1	1	0	46



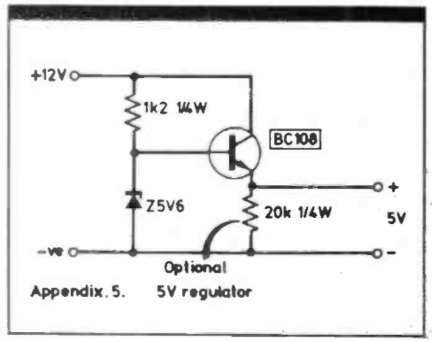
Appendix 3. Basic block diagram of dedicated device.

The BCD format shown is a 7 bit code but obviously by using two columns only in the left hand group* a 6 bit code counting 0-1, 10-19, 20-29, and 30-39 could be used ie a total of 40 lines using 0 as a signal line ie absence of all signals or a No.

Many other forms of binary code are in use but the ones shown are most commonly used. The so-called Random Code is a selective code used in certain devices only as a signalling technique rather than a significator technique and is actually only semi random.

From the above it is apparent that signalling is either by an on or off situation and can be effected by simple switching techniques. This is the principle by which the programmed instructions are issued to the phase lock loop devices.

For similicity of explanation the first table above is shown as reading left to right. It is more conventional to present the table reading right to left as shown in the second table and in **Fig. 15.** ●



Appendix 5. 5V regulator