CB CONVERSIONS

Part Two

How to modify the Binatone Route 66 rig for 10 metre amateur operation

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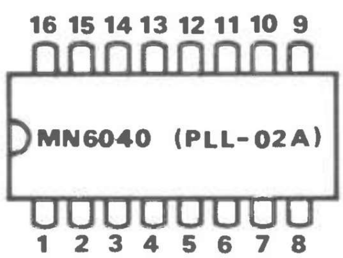
The converted CB had been working in my shack for a few days when the squelch of the set was suddenly lifted and the receiver sprung to life with some strange phrases such as 'Keep the pedal to the metal, have a good day today and a better day tomorrow', which obviously did not belong to amateur radio. The interfering signal remained irrespective of the channel selected. A glance out of the front window revealed a car parked across the road with the driver engaged in a conversation on his radio telephone. Further investigations revealed that the driver was operating a CB rig on channel 4, 27.63125MHz.

Fig 6 PLL02 pin connections



IC-4 Pin No	MN6040 (PLL-02A)
1	Vdd
2	Signal frequency input
3	Reference frequency input
4	Reference divider ratio exchange
5	Phase detector output
6	Lock detector output
7	P8 Programable counter preset input
8	P7 Programable counter preset input
9	P6 Programable counter preset input
10	P5 Programable counter preset input
11	P4 Programable counter preset input
12	P3 Programable counter preset input
13	P2 Programable counter preset input
14	P1 Programable counter preset input
15	P0 Programable counter preset input
16	Ground

The first mixer of the modified CB rig was being injected with a fixed signal which was producing an IF frequency of 10.695MHz. On receive the only fixed frequency within the set is the PLL loop down-mixer crystal oscillator, operating on 38.325MHz. If this frequency is being injected into the receiver first mixer the resulting receiver frequency will be 38.325 minus 10.695 which equals 27.63MHz, only 1.25kHz away from channel 4. An important lesson has been learnt here. When modifying CB rigs always ensure that any changes in internal oscillator frequencies will not, if they find their way into the receiver first or second mixer, cause problems.

How do we overcome this? Additional screening was placed around the oscillator circuit and the supply feed to the oscillator was de-coupled to minimise stray radiation, but in the end this did not solve the problem. The only remaining possibility was to change the frequency of the down-mixer crystal oscillator and compensate by changing the value of the divide by N counter in the PLL chip. This is accomplished by changing the logic on the programme lines of the PLL chip.

An examination of the circuit diagram in *Figure 2* and the pin functions of *Figure 5* revealed that programme line P7, pin 8 is permanently connected to the PLL chip supply voltage, ie at logic level 1, and that programme line P8, pin 7 is permanently connected to ground, logic level 0. It is therefore possible to alter these two programme lines to give different divide by N values. It would be more involved to alter the programme code of the channel select switch (see later) and therefore it was decided to experiment with the two programme lines, P7 and P8.

Change of programme code

Programme lines P7 and P8 can be modified by cutting the printed circuit track to programme lines P7 and P8, which are pins 7 and 8 of IC4.

The first experiment conducted was to put P7 and P8 at logic level 0, that is to earth pins 7 and 8 of IC4. On channel 30 the divide by N number will be 69, see *Figure 7a*. Under lock condition, F_{in} on pin 2 will be 69 × 10kHz = 690kHz. Therefore, the difference on frequency between the VCO and down-mixer crystal oscillator frequency will only be 690kHz. I felt that Q of the output tuned circuit of the down-mixer was not sufficient to prevent the PLL chip being controlled by an unclear signal at F_{in} which could confuse the loop operation.

Fig 7a Truth table for programme code with P7 and P8 at logic level 0

	Channel select switch							Fixed		
	P0	P1	P2	P3	P4	P5	P6	P7	P8	
	2^0	2^1	2^2	2^3	2^4	2^5	2^6	2^7	2^8	
	1	2	4	8	16	32	64	128	256	
Logic code	1	0	1	0	0	0	1	0	0	
Binary value to give divide by N number	1		4				64			=1+4+64=69

Fig 7b Truth table for programme code with P7 and P8 at logic level 1

	Channel select switch							Fixed		
	P0	P1	P2	P3	P4	P5	P6	P7	P8	
	2^0	2^1	2^2	2^3	2^4	2^5	2^6	2^7	2^8	
	1	2	4	8	16	32	64	128	256	
Logic code	1	0	1	0	0	0	1	1	1	
Binary value to give divide by N number	1		4				64	128	256	=453

Fig 7c Truth table for programme code with P7 at logic level 0 and P8 at logic level 1

	Channel select switch							Fixed		
	P0	P1	P2	P3	P4	P5	P6	P7	P8	
	2^0	2^1	2^2	2^3	2^4	2^5	2^6	2^7	2^8	
	1	2	4	8	16	32	64	128	256	
Logic code	1	0	1	0	0	0	1	0	1	
Binary value to give divide by N number	1		4				64		256	=325

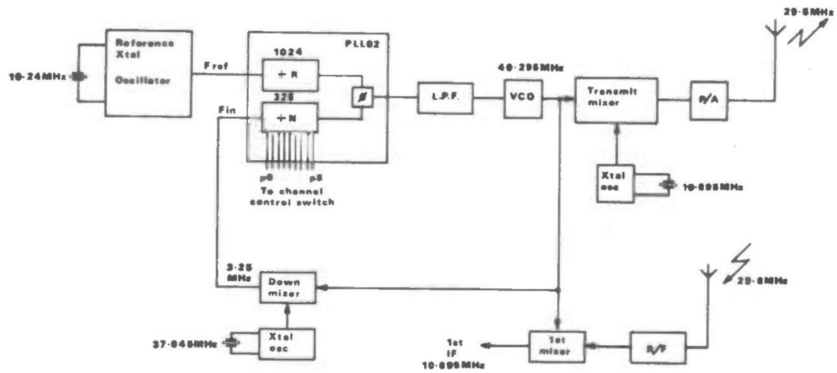


Fig 8 *Block diagram of final modified rig operating on channel 30*

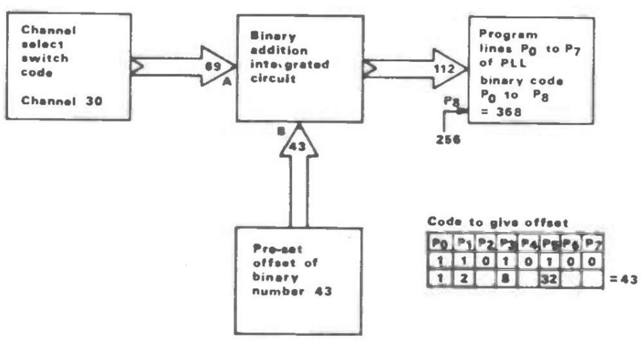


Fig 9 *Changing the binary value of the channel select switch by using binary addition*

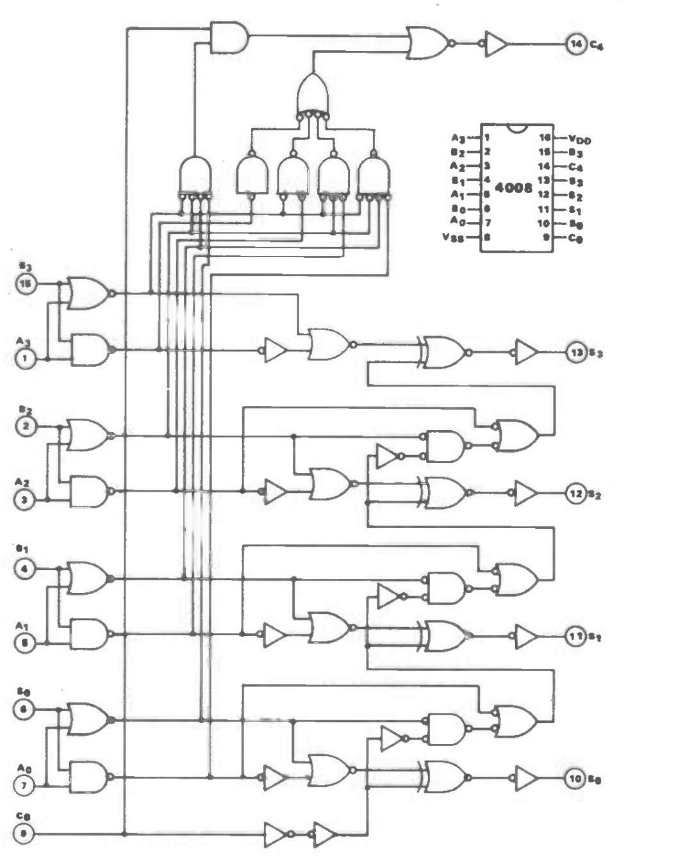


Fig 10 *The circuit configuration and pin out functions of the 4008 integrated circuit*

The second experiment was to put P7 and P8 at logic level 1, that is to connect pins 7 and 8 at the supply voltage to IC4. The resulting divide by N number for channel 30 will be 453 (*Figure 7b*), resulting in an F_{in} frequency of 453 × 10kHz = 4.53MHz. The VCO frequency for channel 30 will remain at 40.295MHz and therefore the frequency of the down-mixer crystal oscillator will be 40.295 − 4.53 = 35.765MHz. Any possible receiver interference problem will occur on 35.765−10.695 = 25.07MHz; a frequency well away from public use and the likelihood of local interference. I did not favour this as a solution because the frequency of F_{in} is approaching the upper frequency limits of the PLL02 chip.

The third experiment involved putting P7 at logic level 0 and P8 at logic level 1. The resulting divide by N number for channel 30 will be 325 (*Figure 7c*). The corresponding value of F_{in} will be 3.25MHz, well within the operating characteristics of the PLL02 chip. The frequency of the down-mixer oscillator will be 40.295 − 3.25 = 37.045MHz. The receiver interfering frequency will be 37.045 − 10.695 = 26.35MHz. Again away from any frequency likely to be used locally. The alignment procedures are identical to that described earlier. The other corresponding channels will remain with an offset of 10kHz between channels because the divide by R network and reference frequency remain unchanged, so that the divide by N value changes by a factor of 1 between each consecutive channel. A block diagram of the final modified rig is shown in *Figure 8*.

Binary addition

For those of you born in the Northern Hemisphere, who consider spending £5.50 on a single crystal to convert a CB rig to the 10 metre FM band expensive, then a possible solution would be to use binary addition on the programme lines to the PLL chip.

Let us consider the unmodified rig operating on channel 30, the block diagram of which is shown in *Figure 1*. From earlier discussions, for the set to operate on 29.6MHz the VCO needs to operate at a frequency of 40.295MHz. The down-mixer oscillator will continue to operate at 36.61625MHz. I strongly recommend that the additional circuit shown in *Figure 4* should be constructed, as I experienced problems in ensuring that the crystal oscillator shown in the circuit diagram of *Figure 2* continued to operate. The resulting output from down-mixing will produce an F_{in} of 3.67875MHz, corresponding to a divide by N number of 3.67875MHz divided by 10kHz which equals 367.875.

Ha! We have a problem. It is not possible to have a divide by N number which is not a whole number. Therefore, if we make the divide by N number equal to 368, this will produce an F_{in} of 3.68MHz. The VCO will be operating on 36.61625 +

3.68 = 40.29625MHz, which will produce an operating frequency of 40.29625 + 10.695, which equals 29.60125MHz, 1.25kHz higher than the required frequency. This can be partially corrected by adjusting the trimming of the down-mixer crystal oscillator.

The main problem confronting the constructor is how he can achieve a programme code of 368 for channel 30 and still maintain the required operating channel switch codes to maintain an offset of 10kHz between consecutive channels. First, we must examine how the binary number is obtained in the original unmodified set. For example, on channel 30, in *Table 1*, the channel change switch provides binary 69 to the PLL integrated circuit programme lines P0 to P6, that is P0, P2, and P6 at logic level 1. Programme line P7 is permanently connected to the positive supply and is therefore at logic level 1, and programme line P8 is grounded to give logic level 0. Therefore, P7 contributes 128 to the programme code binary number to give an overall programme code of 69 plus 128, which equals 197, the divide by N number required.

For the modified rig operating on channel 30 (*Figure 8*), we require a divide by N number of 325 which is achieved when the programme code is 325 binary. To obtain this higher binary number it is necessary to put P7 at logic level 0 and make P8 logic level 1. The binary code now available to the programme lines will be 69 plus 256 which equals 325, only 43 short of the required binary number of 368. We need to find some device that can be inserted between the channel change switch and the inputs of the programme lines of the PLL chip, to permanently increase the channel switch codes by 43 irrespective of the channel selected. The device to use is called a binary adder.

Figure 8 shows the use of a binary adder integrated circuit. The programme code generated by the channel switch is fed directly into the binary adder on input line A. The fixed binary code of 43 which is to be added to the channel switch code is entered into the binary adder on input lines B. The binary adder adds together the binary inputs on lines A and B and presents the addition onto the input lines, which are directly connected to the programme lines P0 through to P7 of the PLL integrated circuit. On channel 30 the binary code from the channel switch, which is 69, is added to the fixed binary code of 43 to produce a binary code of 112. This is presented to the programme lines P0 to P7 of the PLL integrated circuit. Programme line P8 is now permanently at logic level 1 and therefore the overall binary code presented to the programme lines of the PLL integrated circuit will be 112 plus 256, which equals 368, the required binary number for channel 30.

The binary adder integrated circuit selected for the job is the Motorola 4008, which is a four bit binary full adder with

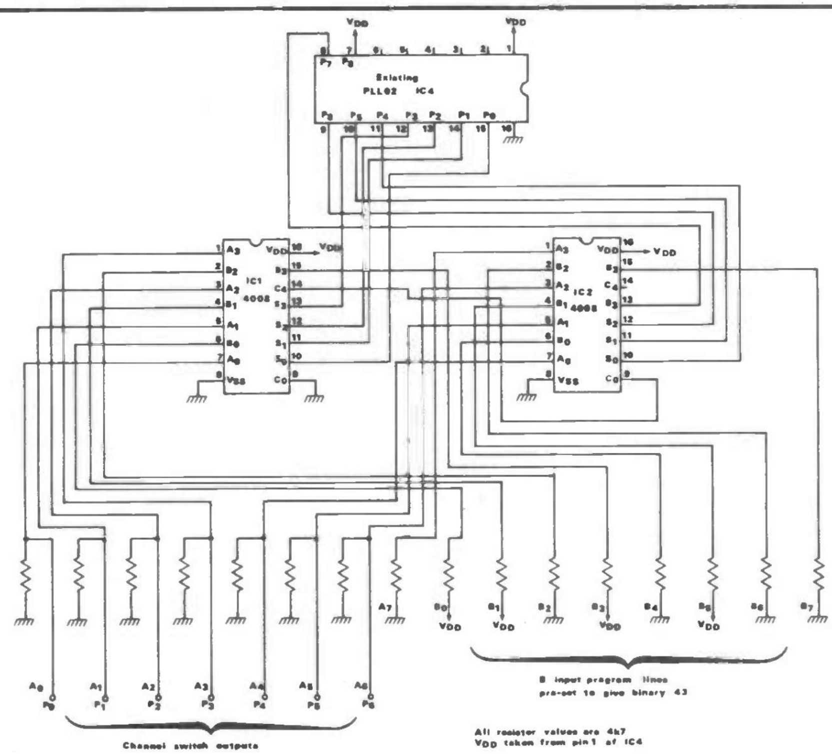


Fig 11 *The full binary adder circuit interposed between the channel switch and the PLL IC*

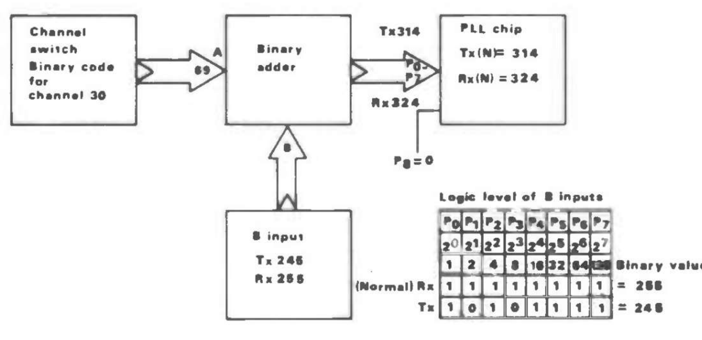


Fig 12 *Using binary addition to achieve frequency shift for repeater working*

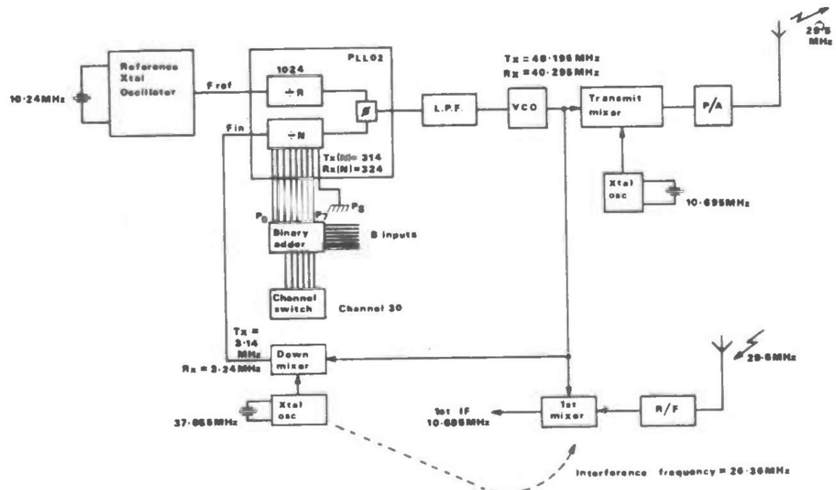


Fig 13 *Block diagram of modified rig tuned to channel 30, incorporating frequency shift for repeater working*

	P0	P1	P2	P3	P4	P5	P6	P7	P8	Binary value
	2^0	2^1	2^2	2^3	2^4	2^5	2^6	2^7	2^8	
	1	2	4	8	16	32	64	128	256	511
(1)	0	0	1	0	0	0	1	0	1	324
(2)	0	0	1	1	1	0	0	0	1	284
(3)	0	0	1	0	1	1	1	1	0	244
(4)	0	0	1	1	0	0	1	1	0	204
(5)	0	0	1	0	0	1	0	1	0	164

PPL02 programme line truth table channel 30

	B0	B1	B2	B3	B4	B5	B6	B7	Binary value
	2^0	2^1	2^2	2^3	2^4	2^5	2^6	2^7	
	1	2	4	8	16	32	64	128	255
(1)	1	1	1	1	1	1	1	1	255
(2)	1	1	1	0	1	0	1	1	215
(3)	1	1	1	1	0	1	0	1	175
(4)	1	1	1	0	0	0	0	1	135
(5)	1	1	1	1	0	0	1	0	95

B input truth table

Band	Frequency range		
	Chan 1	Chan 30	Chan 40
(1)	29.31MHz	29.60MHz	29.70MHz
(2)	28.91MHz	29.20MHz	29.30MHz
(3)	28.51MHz	28.80MHz	28.90MHz
(4)	28.11MHz	28.40MHz	28.50MHz
(5)	27.51MHz	28.00MHz	28.10MHz

Table 2 *Truth table for the programme codes for the PLL02 chip and the B inputs*

two four bit data inputs, A0 to A3, and B0 to B3, a carry input C0 four sum outputs, S0 to S3, and a carry output C4. The 4008 incorporates full look ahead across 4 bits to generate the carry output C4. This minimises the necessity for extensive look ahead and carry cascading circuits. The circuit configuration and pin out functions are shown in *Figure 10*.

To achieve full binary addition, two 4008 ICs will be required. The full circuit diagram of the binary adder circuit is shown in *Figure 11*. The input programme lines for both IC1 and IC2 are grounded through 4.7kohm resistors to ensure that their outputs are at logic level 0 when not being used. The logic outputs of the channel change switch are connected to A0 through to A3 of IC1 and A0 through to A2 of IC2. A3 of IC2 is not used and is grounded via a 4.7kohm resistor.

The B inputs for both binary adder ICs are fed via a 4.7kohm resistor to either VDD or ground to achieve the binary value of 43. The carry output of IC1 is connected to the carry input of IC2 to achieve full carry over between the two binary adder integrated circuits. The carry input of IC1 is not used and is grounded to ensure that noise cannot trigger the input to give an incorrect output code. The carry output of IC2 is not used and pin 14 is left open circuit.

At a VDD of approximately 10V each, 4008 consumes about 1.4 milliamps and therefore it is acceptable to use the same voltage rail which feeds the PLL chip IC4.

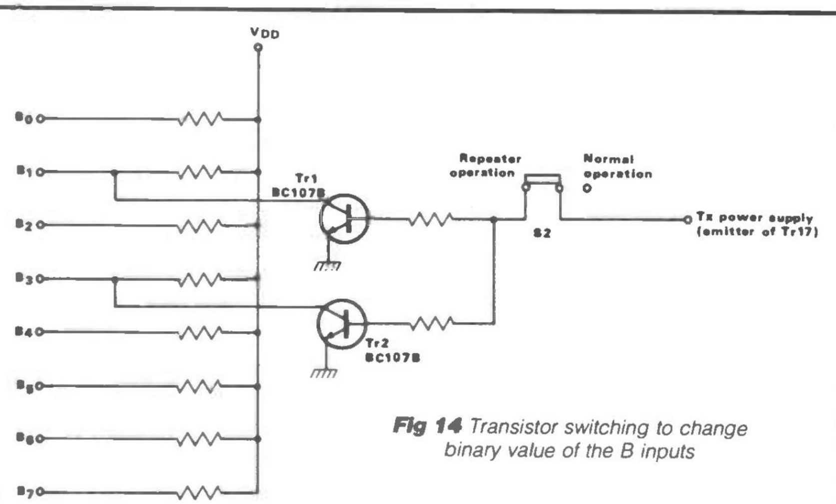


Fig 14 *Transistor switching to change binary value of the B inputs*

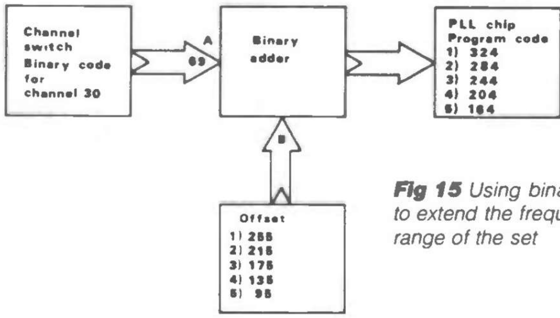


Fig 15 *Using binary addition to extend the frequency range of the set*

Construction

The two binary adder integrated circuits, IC1 and IC2, are mounted on a small piece of Veroboard. It is wise to use an IC holder and complete the soldering before inserting the two ICs to avoid damaging them, as we are dealing with CMOS logic. The resistors are also mounted on Veroboard and ribbon cable is used to interconnect to the set printed circuit board. If difficulty is experienced putting the set on frequency because the down-mixer crystal oscillator will not shift sufficiently in frequency, it is worth trying again with the divide by N number reduced by 1. This can be achieved by removing VDD from B0 and connecting it to ground. Remember that the VCO will also require to be set up as previously described.

When the final tuning has been accomplished the Veroboard is insulated with PVC tape to ensure that it does not come into contact with the other components in the set.

Providing repeater shift

Having now experienced the 'delights' of binary addition, it is possible to make use of this technique to provide additional facilities. For example, when the sunspot cycle becomes favourable for DX working on 10 metres, working through the repeaters of other countries can be very enjoyable. To achieve this facility within the modified set we need to ensure that the transmit frequency is 100kHz below the receive frequency. It is therefore necessary to change the value of the divide by N number between transmit and receive. The only other way of achieving the same result is to keep the same divide by N number between transmit and receive and use another crystal in the down-mixer oscillator which is a more expensive way of providing this facility.

With the transmitter operating 100kHz below the receiver frequency the divide by N number on receive will be higher than that on transmit. If we make the B inputs to the binary adder all at logic level 1 (*Figure 12*), the resulting binary number will be 255. On channel 30 the binary number produced by the channel change switch will be 69, which is fed to the A inputs of the binary adder. The binary adder output will be 69 plus 255 which equals 324. Therefore, the resulting divide by N number will be 324. The frequency of F_{in} will be 324 × 10kHz which equals 3.24MHz.

From previous examples, we know that the VCO will be operating at 40.295MHz on channel 30 and therefore the frequency of the down-mixer crystal oscillator will be 40.297MHz – 3.24MHz, which equals 37.055MHz. If this frequency should find its way into the receiver first mixer, the interfering frequency will be 37.055MHz – 10.695MHz which equals 26.36MHz, this frequency being well away from any possible locally generated transmissions. On transmit the frequency must be 100kHz below the receive frequency and therefore on channel 30 will be operating at 29.5MHz. The VCO requires to operate at a frequency of 29.6MHz – 10.695MHz which equals 40.195MHz. The frequency of F_{in} will be 40.195MHz – 37.055MHz which equals 3.14MHz.

The required divide by N number to produce a frequency of 10kHz to the input of the phase detector to maintain the loop in a locked condition will be 3.14MHz divided by 10kHz, which equals 314. The binary number on the inputs of the programme lines will be 314.

Figure 13 shows the block diagram of the modified rig giving the frequency relationships existing within the rig. On transmit the output of the binary adder will be 324. The binary value of the B inputs to achieve this value will be 314 – 69 which equals 245. To achieve a binary value of 245 we require to make all the B inputs at logic level 1, with the exception of P1 and P3 which are placed at logic level 0 *(Figure 12)*. Therefore, to obtain the 100kHz frequency shift, we only need to change the logic level of two of the B inputs from logic level 1 to 0.

We can use the same circuit configuration of *Figure 11* with the exception that all the B inputs are held at logic level 1 by connecting all the resistors to VDD. On transmit we require to ground the inputs of P1 and P3 which can be achieved using transistors, as shown in *Figure 14*. On transmit the bases of Tr1 and Tr2 are connected to the transmit voltage rail, which causes Tr1 and Tr2 to conduct heavily and ground P1 and P3. The front panel switch to select PA or CB, S2, can be used to select repeater operation as shown in *Figure 14*. The two transistors were mounted on the same piece of Veroboard containing the binary adder ICs. The base current of the two transistors is limited by 4.7kohm resistors and the trigger voltage is taken from the emitter of Tr17, the transistor regulator and switch to supply the transmitter when the mic button is pressed.

The frequency range

Binary addition can again be used, this time to extend the frequency range of the set. For example, the set may be used as an exciter to obtain operation on the 2 metre band. If this is the case, the set must be capable of operating over a bandwidth of 2MHz between 28MHz to 30MHz.

Let us assume that on Band 1 channel 30 will remain the calling frequency of 26.6MHz, and that we will adopt the two 4008s approach with all the B inputs at logic level 1. From *Table 2*, the binary value with B0 to B7 all set at logic level 1 will be 255. The output of the binary adder (*Figure 15*) will result in a binary value of 68 + 255 which equals 324. F_{in} will be 324 × 10kHz, which equals 3.24MHz. On channel 30, the VCO will be operating at a frequency of 29.6MHz plus 10.695MHz, which equals 48.295MHz. The down-mixer crystal oscillator must operate at a frequency of 40.295MHz – 3.24MHz, which equals 37.055MHz, the same frequency as in the previous example.

To obtain complete coverage of the amateur ten metre band, you will observe from *Table 2* that on Band 2 at channel 30 the operating frequency of the set will be 29.2MHz, a drop of 40kHz from channel 30 on Band 1. From *Figure 17* the VCO will be operating at a frequency of 29.2MHz plus 10.695MHz, which equals 39.895MHz. F_{in} will be 39.895MHz – 37.055MHz, which equals 2.84MHz. The resulting divide by N number will be 2.84MHz divided by 10kHz, which equals 284, also corresponding to the binary number appearing on the input programme lines to the PLL chip. From *Figure 15* the B binary code required will be 284 – 69, which equals 215. The truth table is given in *Table 2*. The same calculation exercise is continued for the remaining 3 bands.

The output of the binary adder is connected to programme lines P0 through to P7. It will be noted from *Table 2* that programme line P8 does not remain at logic level 1 throughout the 5 bands, and therefore cannot be permanently connected to VDD. However, a close examination of the B inputs of the binary adder reveal that B4 has a similar bit pattern per band as for P8, and therefore there is nothing stopping one connecting B4 directly to P8.

The next remaining problem is how we obtain the various logic codes on the B

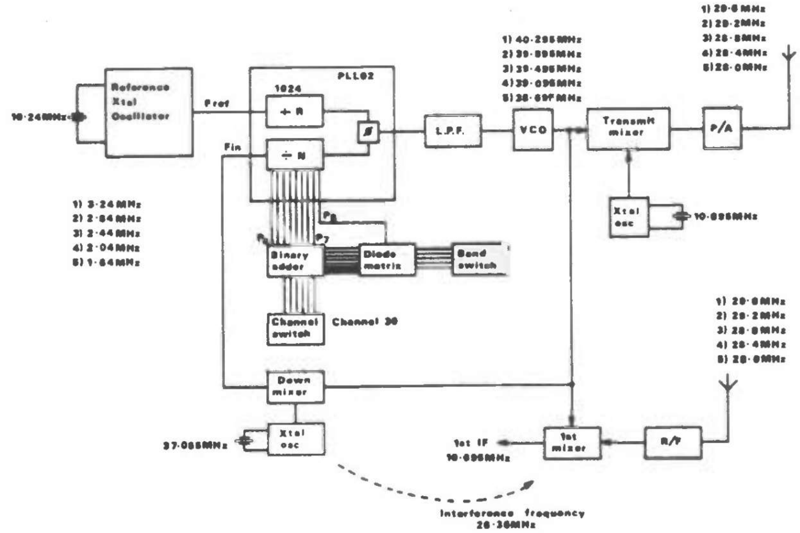


Fig 16 *Block diagram of the modified rig tuned to channel 30, which will tune over 5 bands to cover from 27.51MHz to 29.7MHz*

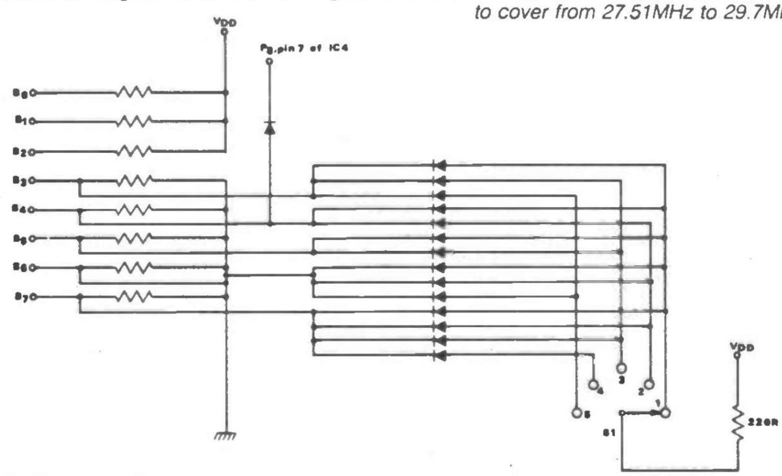


Fig 17 *Diode switching to achieve the required binary code for the B inputs of the binary adder*

input to the binary adder for each individual band. Again, a close examination of the inputs reveals that B0, B1 and B2 always remain at logic level 1 and therefore can be permanently connected to VDD. However, B2 through to B7 change state from one band to another. In the previous example we used transistor switching to achieve the change in logic levels, but this would prove unsuitable in this situation. The answer to the problem is to put the B inputs B3 through to B7 at logic level 0 through 4.7kohms resistors to ground and use diode switching as a means of changing the logic level of the individual B inputs.

Diode switching

Figure 17 shows the arrangement of diode switching. The band switch S1 connects VDD via a diode to prevent back feeding to the various B inputs, as shown by the truth table for the B inputs in *Table 2* . This method uses only 14 switching diodes, with B4 connected to P8 via an additional switching diode. The diode matrix was constructed on a separate piece of Veroboard and then wired to the band switch which is mounted on the front panel of the set, and also wired to the Veroboard containing the two binary adder ICs. The B inputs B0, B1 and B2 are connected to VDD via 4.7kohm resistors, while the remaining B inputs are connected to ground via similar resistors.

The VCO in this set is operating at a frequency of around 40MHz and therefore with the existing values of tuned L and C is capable of operating over a frequency range of 2MHz, whereas in other sets with a VCO operating at around 17MHz the ratio of the tuned L and C in the VCO circuit will have to be adjusted to increase the VCO to operate over a bandwidth of 2MHz.

Conclusions

The Binatone Route 66 transceiver model 01/8538 is relatively easy to convert for use on the 10 metre band. However, there are a number of pitfalls to be avoided.

The PLL02 PLL chip is not capable of operating at a frequency of F_{in} greater than approximately 4.5MHz, although the programme codes with a reference oscillator operating at 10.24MHz will permit an F_{in} with all programme lines at logic level 1 of 5.11MHz.

Secondly, to avoid any possible interference from the UK Citizens Band, the down-mixer crystal oscillator must be selected to avoid the receiver first mixer mixing these unwanted frequencies. Therefore, avoid a down-mixer crystal oscillator frequency varying from 38MHz up to 38.7MHz.

Thirdly, before completing the frequency alignment of the set, ensure that the reference oscillator is operating at 10.24MHz. If not, adjust the trimmer VC2. Also, check on transmit that the transmitter crystal oscillator is oscillating at 10.695MHz; again if not adjust trimmer VC1.

The modified set with the down-mixer oscillator operating on 37.045MHz has been working in the shack for the past three months without any problem and works well on local nets. Unfortunately, the sunspot activity is not very good and no opportunity has arisen to try working any DX stations. The Binatone transceiver is probably one of the cheapest sets to convert to 10 metres, approximately £2.00 if you use binary addition and £5.50 if the down-mixer crystal is changed.

I hope that this article will have kindled your interest in 10 metres and will not only assist you to modify the Binatone rig but any CB rig containing the versatile PLL02 phase locked loop integrated circuit. REW